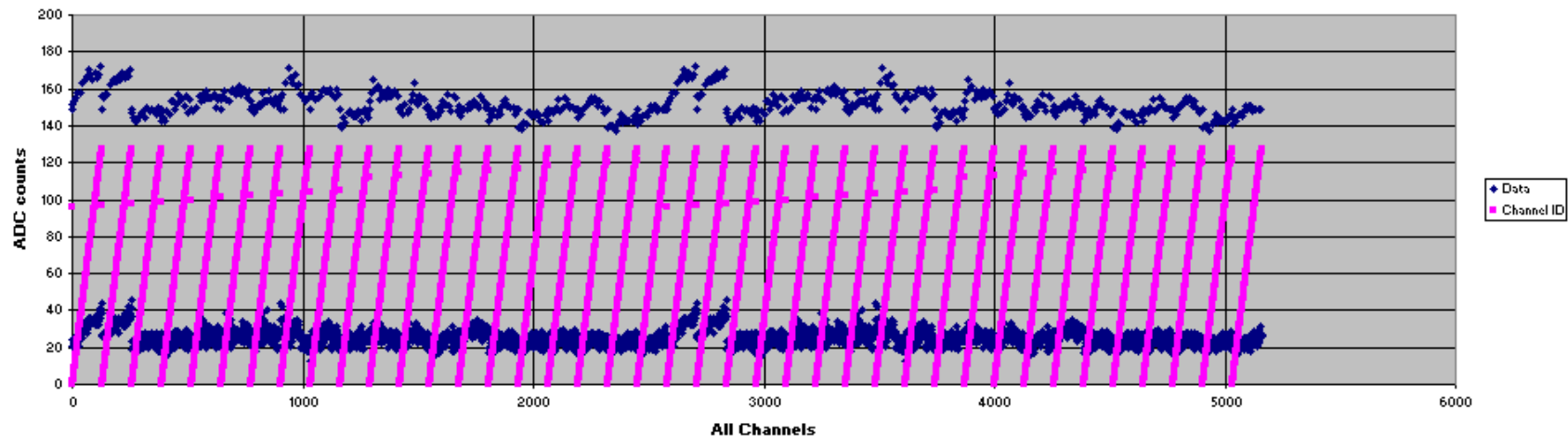# readout errors on SaSeq test stands

readout with 4 full chains has error rate
4 ev./200k events. typical failure:

**full readout, RTPS: failure after 159k events - slave was read instead of master**



wrong chip IDs in first 20 chips! (everything else fine)
➡ standard spreadsheet does not see this error

## explanation for this type of error

VME bus errors during DMA data transfer SaSeq $\longrightarrow$ Bit3

➡ data transfer fails

➡ spreadsheet sees previous event still in memory

➡ repeated events (1 SaSeq), resp.

identical data in master/slave chains (2 SaSeqs)

Recovery times after each VME error:

full chain test stand: 4 faulty events before recovery

burn-in test stand: 1800 faulty events before recovery!

Standard spreadsheet ignores VME errors

$\longrightarrow$ repeated events!

# VME bus error overview

| test stand | Sara's full chain | Sara's purple crd | Burn-in purple crd | Cecil's purple crd |
|---|---|---|---|---|
| errors in DMA mode | YES | YES | YES | ??? |
| errors in non-DMA | YES | YES | NO | NO |

Cecil's test stand cannot do DMA

NO error means none in 5–10 million events

## readout errors: conclusion

preliminary conclusion: probably two effects

● minor problem with Bit3 DMA mode?
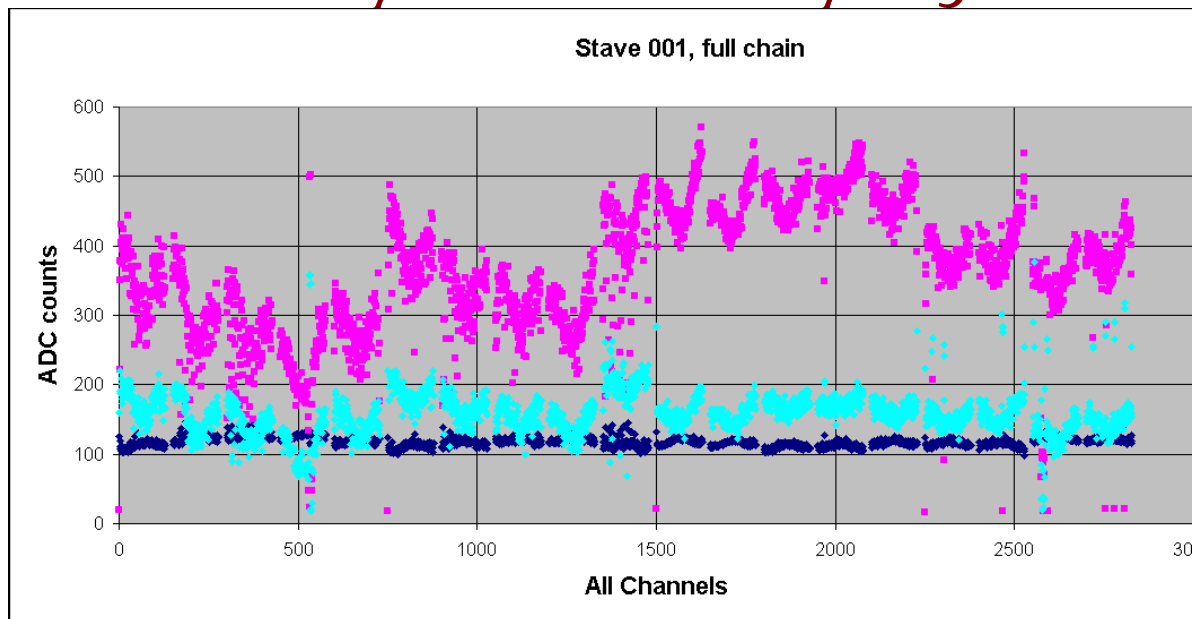
● defective crate and/or Bit3 in Sara's test stand?

in any case:

besides VME bus errors, not a single readout error seen
in millions of events with 4 full chains!

➡ ready for the "big thing" (the electrical stave)
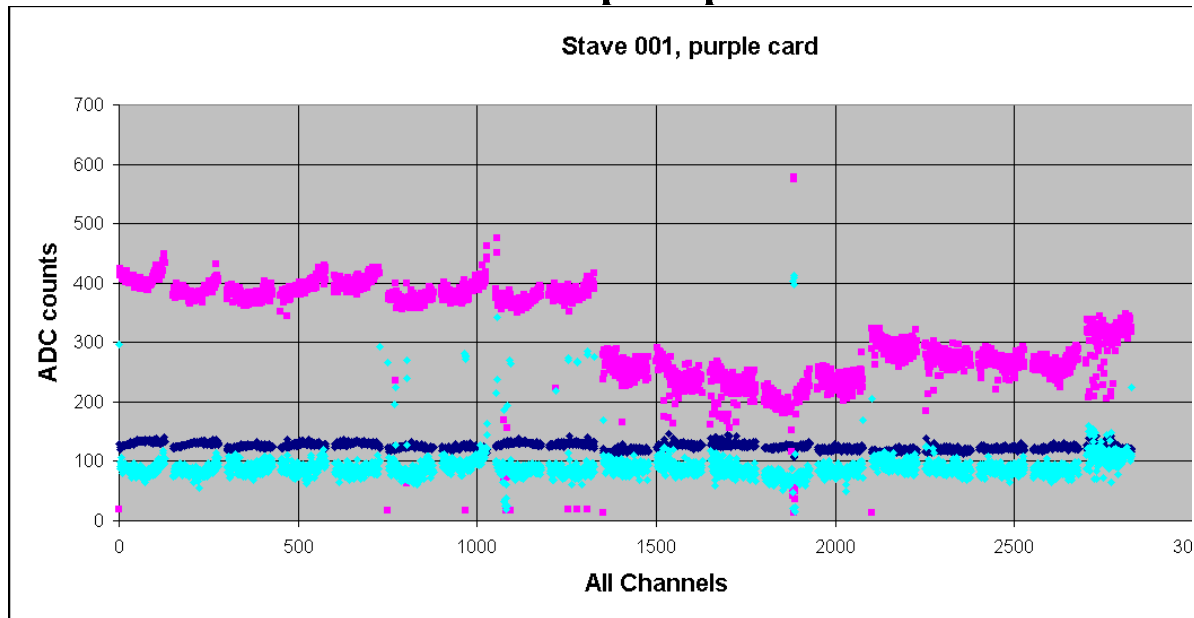
## first look into stave readout

first readout of 1/2 electrical stave
(10-10 axial and 20-20 axial mounted on stave core)
no HV bias yet! no Faraday cage!



Stave 001, full chain

well, at least it works… (no readout errors/1000 events)

# first look into stave readout (contd.)

## stave readout with purple card:



- about 1% failed events (not yet investigated)
- one hybrid occasionally reads all channels 0 ADC

## conclusions

work in progress...

but the readout is in very good shape!